IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1-6. (Cancelled)

7. (Currently amended) A method for managing power consumption in a computer system, comprising:
placing said computer system in power management mode;
requesting removing power from a memory device coupled to said computer system;
allocating a second memory in said computer system;
removing power from said memory device; and
directing access intended for said memory device to said second memory while power is removed from said memory device;
wherein said memory device and said second memory each comprises a plurality of addressable locations, and wherein for each address location in said second memory, there are a plurality of corresponding address locations in said memory device.

8. (Currently amended) The method of claim 7, further comprising executing a process that includes instructions for accesses to said memory device, said accesses being directed to said second memory.

9. (Currently amended) The method of claim 8, further comprising reading data from said second memory to allow said process to continue running.

10. (Currently amended) The method of claim 8, further comprising writing data generated from said process to said second memory.

11. (Original) The method of claim 7, further comprising detecting an idle state of

said computer system, and wherein said requesting removing power is responsive to said detection of said idle state.

12. (Original) The method of claim 7, further comprising determining whether there has been external activities at said computer system for a predetermined time.

13. (Original) The method of claim 12, wherein said external activities comprise activities at a keyboard or a mouse coupled to said computer system.

14. (Currently amended) The method of claim 7, further comprising:
restoring power to said memory device;
restoring device state to said memory device; and
updating said memory device.

15. (Currently amended) The method of claim 14, further comprising releasing said second memory and restoring a first mapping such that data is mapped to said memory device.

16. (Original) The method of claim 14, wherein said updating comprises redrawing windows on a display device.

17-19. (Cancelled)

20. (Currently amended) A method for power managing a framebuffer coupled to a computer system, comprising directing access requests intended for said framebuffer to a memory in the [[a]] computer system, while said computer system is in a power management mode and said framebuffer is powered off, wherein said framebuffer and said memory each comprises a plurality of addressable locations, and wherein for each address location in said memory, there are a plurality of corresponding address locations in said framebuffer.

21. (Currently amended) The method of claim 20, wherein a specified constant value is stored in each of the plurality of addressable locations in said memory, and wherein the constant value is read back when the framebuffer is powered back on [[said framebuffer and said memory each comprises a plurality of addressable locations, and wherein there is a unique address location in said memory corresponding to each address location in said framebuffer]].

22. (Original) The method of claim 20, wherein said framebuffer and said memory each contains a plurality of addressable locations, and wherein there are fewer addressable locations in said memory than addressable locations in said framebuffer.

23. (Currently amended) The method of claim 20[[22]], wherein accesses to all addressable locations in said framebuffer are directed to a single addressable location in said memory.

24. (Cancelled)

25. (Currently amended) A computer system with power management capabilities, comprising a power management circuit capable of directing access intended for a memory device coupled to said computer system to a second memory in said computer system when said computer system is in a power management mode and said memory device is powered off, wherein said memory device and said second memory each comprises a plurality of addressable locations, and wherein for each address location in said second memory, there are a plurality of corresponding address locations in said memory device.

26. (Currently amended) The computer system of claim 25, wherein said power management circuit comprises:

a server for handling communication between a process and [[a]] the memory device;

a device driver for accessing said memory device; and

a power manager for setting a power level of said memory device.

27. (Currently amended) A computer system with power management capability, comprising:

a display device;

a framebuffer associated with said display device; and

a virtual framebuffer, wherein access to said framebuffer is directed to said virtual framebuffer when said computer system is in power management mode and said framebuffer is powered off;

wherein said framebuffer and said second memory each comprises a plurality of addressable locations, and wherein for each address location in said virtual framebuffer, there are one or more corresponding address locations in said framebuffer.

28. (Cancelled)

29. (Currently amended) A computer readable medium which stores program instructions for [[implementing an instruction set for directing]] power management, wherein the program instructions are executable by a processor to:

direct access intended for a memory device to a second memory [[space]] during power management mode of a computer system coupled to said memory device and when said memory device is powered off;

wherein said memory device and said second memory each comprises a plurality of addressable locations, and wherein for each address location in said second memory, there are a plurality of corresponding address locations in said memory device.